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Design Environment User Guide. For more information about using the Spectre circuit simulator with Verilog-A, see the Verilog-A Language Reference manual. If you want to see how SpectreRF is run under the analog circuit design environment, read SpectreRF Simulation Option User Guide.

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In the arena of parasitic-aware design of CMOS RF circuits, efforts are aimed at the realization of true single-chip radios with few, if any, off-chip components. The parasitic-aware RF circuit synthesis techniques described in this book effectively address critical problems in this field.

VLSI for Wireless Communication, Second Edition, an advanced level text book, takes a system approach starting with an overview of the most up to date wireless systems and the transceiver architecture available today. Wireless standards are first introduced (updated to include the most recent 3G/4G standards in the second edition), and translates from a wireless standard to the implementation of a transceiver. This system approach is particularly important as the level of integration in VLSI increases and coupling between system and component design becomes more intimate. VLSI for Wireless Communication, Second Edition, illustrates designs with full design

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examples. Each chapter includes at least one complete design example that helps explain the architecture/circuits presented in this text. This book has close to 10 homework problems at the end of each chapter. A complete solutions manual is available on-line. VLSI for Wireless Communication, Second Edition, is designed as a primary text book for upper-undergraduate level students and graduate level students concentrating on electrical engineering and computer science. Professional engineers and researchers working in wireless communications, circuit design and development will find this book valuable as well.

High-speed, power-efficient analog integrated circuits can be used as standalone devices or to interface modern digital signal processors and micro-controllers in various applications, including multimedia, communication, instrumentation, and control systems. New architectures and low device geometry of complementary metaloxidesemiconductor (CMOS) technologies have accelerated the movement toward system on a chip design, which merges analog circuits with digital, and radio-frequency components.

This work covers the design of CMOS fully integrated low power low phase noise voltage controlled oscillators for telecommunication or

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datacommuni- tion systems. The need for low power is obvious, as mobile wireless telecommunications are battery operated. As wireless telecommunication systems use oscillators in frequency synthesizers for frequency translation, the selectivity and signal to noise ratio of receivers and transmitters depend heavily on the low phase noise performance of the implemented oscillators. Datacommunication s- tems need low jitter, the time-domain equivalent of low phase noise, clocks for data detection and recovery. The power consumption is less critical. The need for multi-band and multi-mode systems pushes the high-integration of telecommunication systems. This is o?ered by sub-micron CMOS feat- ing digital ?exibility. The recent crisis in telecommunication clearly shows that mobile hand-sets became mass-market high-volume consumer products, where low-cost is of prime importance. This need for low-cost products - livens tremendously research towards CMOS alternatives for the bipolar or BiCMOS solutions in use today.

Modern telecommunication systems are highly complex from an algorithmic point of view. The complexity continues to increase due to advanced modulation schemes, multiple protocols and standards, as well as additional functionality such as personal organizers or navigation aids. To have short and reliable design cycles, efficient

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verification methods and tools are necessary. Modeling and simulation need to accompany the design steps from the specification to the overall system verification in order to bridge the gaps between system specification, system simulation, and circuit level simulation. Very high carrier frequencies together with long observation periods result in extremely large computation times and requires, therefore, specialized modeling methods and simulation tools on all design levels. The focus of Modeling and Simulation for RF System Design lies on RF specific modeling and simulation methods and the consideration of system and circuit level descriptions. It contains application-oriented training material for RF designers which combines the presentation of a mixed-signal design flow, an introduction into the powerful standardized hardware description languages VHDL-AMS and Verilog-A, and the application of commercially available simulators. Modeling and Simulation for RF System Design is addressed to graduate students and industrial professionals who are engaged in communication system design and want to gain insight into the system structure by own simulation experiences. The authors are experts in design, modeling and simulation of communication systems engaged at the Nokia Research Center (Bochum, Germany) and the Fraunhofer Institute for Integrated Circuits, Branch Lab Design Automation (Dresden, Germany).

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In this book, the authors outline detailed design methodology for fast frequency hopping synthesizers for RF and wireless communications applications. There is great emphasis on fractional-N delta-sigma based phase locked loops from specifications, system analysis and architecture planning to circuit design and silicon implementation. The developed techniques in the book can help in designing very low noise, high speed fractional-N frequency synthesizers.

Summarizes cutting-edge physical layer technologies for multi-mode wireless RF transceivers. Includes original contributions from distinguished researchers and professionals. Covers cutting-edge physical layer technologies for multi-mode wireless RF transceivers. Contributors are all leading researchers and professionals in this field.

The book presents design methods for analog integrated circuits with improved electrical performance. It describes different equivalent transistor models, design methods, and fabrication considerations for

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high-density integrated circuits in nanometer CMOS processes, and it analyzes circuit architectures that are suitable for analog building blocks. Highlighting various design challenges, the text offers a complete understanding of architectural- and transistor-level design issues of analog integrated circuits. It examines important trends in the design of high-speed and power-efficient front-end analog circuits that can be used for signal conditioning, filtering, and detection applications. Offers a comprehensive resource for mastering the analysis of analog integrated circuits. Describes circuit-level details of high-speed and power-efficient analog building blocks. Explores design methods based on various MOS transistor models (MOSFET, FinFET). Provides mathematical derivations of all equations and formulas. Emphasizes practical aspects relevant to integrated circuit implementation. Includes open-ended circuit design case studies.

Engineering productivity in integrated circuit product design and development today is limited largely by the effectiveness of the CAD tools used. For those domains of product design that are highly dependent on transistor-level circuit design and optimization, such as high-speed logic and memory, mixed-signal analog-digital interfaces, RF functions, power integrated circuits, and so forth, circuit

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simulation is perhaps the single most important tool. As the complexity and performance of integrated electronic systems has increased with scaling of technology feature size, the capabilities and sophistication of the underlying circuit simulation tools have correspondingly increased. The absolute size of circuits requiring transistor-level simulation has increased dramatically, creating not only problems of computing power resources but also problems of task organization, complexity management, output representation, initial condition setup, and so forth. Also, as circuits of more complexity and mixed types of functionality are attacked with simulation, the spread between time constants or event time scales within the circuit has tended to become wider, requiring new strategies in simulators to deal with large time constant spreads.

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